TITLE

LIQUID CRYSTAL DISPLAY DEVICE WITH A CAPACITANCE-COMPENSATED

STRUCTURE

BACKGROUND OF THE INVENTION

5 **Field of the Invention**

The present invention relates in general to a liquid crystal display device. More particularly, it relates to a liquid crystal display device with a capacitance-compensated structure.

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Description of the Related Art:

Due to the characteristics of thin profile, low power consumption, and lower driving voltage, liquid crystal displays (LCDs) have been widely used in flat panel

15 displays. Owing to dielectric anisotropy and conductive anisotropy of liquid crystal molecules, molecular orientation of liquid crystals can be shifted under an external electric field, such that various optical effects are produced. Generally, the display area of a LCD

20 comprises a plurality of pixel areas and each pixel area further comprises a pair of gate lines (scan line) and a pair of data lines to define a rectangular region. A thin film transistor (TFT), serving as a switching device, and a pixel electrode are disposed in the rectangular region.

25 FIG. 1 is a plane view of the conventional liquid crystal display device. In FIG. 1, the dotted line region indicates a thin film transistor T, which comprises a gate

G, a source S, and a drain D. the gate G extends from a gate line 12 formed by process M1 (first metal layer). A data line 22 and the metal portions of the source S and the drain D are formed by process M2 (second metal layer). The symbol

5   18 indicates a channel protection layer and the symbol 24 indicates a pixel electrode. A gate-drain parasitic capacitor C_{gd} is formed between the gate G and the drain D. A gate-source parasitic capacitor C_{gs} is formed between the gate G and the source S. The capacitances of the gate-drain

10   parasitic capacitor C_{gd} and the gate-source parasitic capacitor C_{gs} are changed when alignment shift occurs after processes M1 and M2. For example, when the second metal layer shifts towards the left side (the source S and the drain D shift toward the left side), the capacitance of the

15   gate-drain parasitic capacitor C_{gd} is increased and that of the gate-source parasitic capacitor C_{gs} is reduced. Conversely, when the second metal layer shifts towards the right side (source S and drain D shift toward the right side), the capacitance of the gate-drain parasitic capacitor

20   C_{gd} is reduced and that of the gate-source parasitic capacitor C_{gs} is increased.

FIG. 2 is an equivalent circuit diagram of the conventional liquid crystal display device. As shown in FIG. 2, the changed capacitance of the gate-source parasitic

25   capacitor C_{gs} does not directly affect the liquid crystal cell 36. The changed capacitance of the gate-drain parasitic capacitor C_{gd}, however, changes the voltage applied to the liquid crystal cell 36. This is because the gate-drain parasitic capacitor C_{gd} is serially connected to

30   the corresponding parallel circuit 36a of the liquid crystal

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cell 36 and the storage capacitor C_{st} (not shown in FIG. 1).
When the thin film transistor T is turned off, the serially
connected gate-drain parasitic capacitor C_{gd} reduces the
voltage on the liquid crystal cell 36, inducing mura effect
5   during operation of the liquid crystal display.

SUMMARY OF THE INVENTION

Accordingly, an object of the invention is to provide a
liquid crystal display device with a capacitance-compensated
10   structure, which can compensate the changed capacitance of
the gate-drain parasitic capacitor when alignment shift
occurs after M1 and M2 processes.   The capacitance-
compensated structure is electrically connected to the gate.
One side of the drain overlaps with the gate and the other
15   side of the drain overlaps with the capacitance-compensated
structure.

Another object of the invention is to provide a liquid
crystal display device with a capacitance-compensated
structure, wherein a parasitic capacitor structure is
20   disposed on the side of the drain without overlapping with
the gate and is electrically connected to the gate.   When
the parasitic capacitance in the overlapping region between
the drain and the gate is changed, the parasitic capacitor
structure can compensate the changed capacitance, so as to
25   substantially maintain the original capacitance of the gate-
drain parasitic capacitor.

According the objects of the invention, a liquid
crystal display device is provided.   The device comprises a
first process layer with a capacitance-compensated structure

and a second process layer. The first process layer comprises a gate line, a gate, and a compensation structure, wherein the gate is electrically connected to the gate line and the compensation structure electrically connects to the

5   gate. The second process layer comprises a data line, a source and a drain. The source and the drain correspond to both sides of the gate, respectively. The source is electrically connected to the data line. The data line is substantially perpendicular to the gate line. The drain has

10   a first side overlapping the gate and a second side overlapping the compensation structure, wherein the first side is opposite to the second side. Moreover, an acceptable alignment shift range exists between the first process layer and the second process layer and the sum of

15   the capacitance of a first parasitic capacitor between the first side of the drain and the gate and a second parasitic capacitor between the second side of the drain and the compensation structure maintains a substantially constant value within the acceptable alignment shift range.

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DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings, given by way of illustration only and

25   thus not intended to be limitative of the present invention.

FIG. 1 is a plane view of the pixel area of the conventional liquid crystal display device.

FIG. 2 is an equivalent circuit diagram of the conventional liquid crystal display device.

FIG. 3A is a plane view of the pixel area of a liquid crystal display device of the invention without any alignment shift between the first metal layer and the second metal layer.

5   FIG. 3B is a plane view of the pixel area of a liquid crystal display device of the invention with alignment shift between the first metal layer and the second metal layer.

FIG. 4 is a cross-section along the line 4-4' shown in FIG. 3B.

10   FIG. 5 is an equivalent circuit diagram of a pixel unit with a C_{gd} capacitance-compensated structure according to the first embodiment of the invention.

FIG. 6 is a plane view of a C_{gd} capacitance-compensated structure according to the second embodiment of the

15   invention.

FIG. 7 is a plane view of a C_{gd} capacitance-compensated structure according to the third embodiment of the invention.

20   **DETAILED DESCRIPTION OF THE INVENTION**

In the invention, a compensation capacitor is provided for compensating the changed capacitance of the gate-drain parasitic capacitor (C_{gd}) due to the alignment shift between the first metal layer (M1) and the second metal layer (M2),

25   thereby ensuring the capacitance of the C_{gd} can maintain a constant value within the acceptable alignment shift range between M1 and M2.

One side of the drain formed by process M2 overlaps with the gate formed by process M1 and the channel

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protection layer. Conventionally, the other side of the drain overlaps with the pixel electrode and does not overlap with any wiring formed by process M1. Moreover, a conductive plug is disposed on the overlapping region to

5   serve as an electrical connection between the pixel electrode and the drain. In the invention, however, a compensation structure overlaps the other side of the drain. Accordingly, when alignment shift occurs after process M2, the overlapping region between one side of the drain and the

10 gate shifts and then the overlapping region between the other side of the drain and the compensation structure also shifts for capacitance compensation. As a result, the original capacitance of the gate-drain parasitic capacitor is changed with a differential capacitance ΔC_1. The

15 overlapping region between the drain and the compensation structure produces a compensative capacitance ΔC_2. Here, the modulus of ΔC_1 is substantially equal to that of ΔC_2. As shown in table 1, when ΔC_1 is positive, ΔC_2 is negative. Conversely, when ΔC_1 is negative, ΔC_2 is positive. That is,

20 $\Delta C_1 + \Delta C_2 \cong 0$ or $|\Delta C_1| - |\Delta C_2| \cong 0$. Accordingly, even if alignment shift between M1 (the first metal layer) and M2 (the second metal layer) occurs, the gate-drain parasitic capacitor (C_{gd}) is not affected.

25   Table 1

Overlapping region (between D and G) Capacitance	ΔC_1	ΔC_2
Increase	$\Delta C_1 > 0$	$\Delta C_2 < 0$

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No changing	$\Delta C_1 = 0$	$\Delta C_2 = 0$
Reduce	$\Delta C_1 < 0$	$\Delta C_2 > 0$

FIGS. 3A and 3B are plane views of a C_{gd} capacitance-compensated structure according to the first embodiment of the invention. FIG. 3A illustrates the case of a pixel area without alignment shift between M1 and M2. FIG. 3B additionally illustrates the case of a pixel area where alignment shift occurs between M1 and M2. Additionally, FIG. 4 is a cross-section along the line 4-4' shown in FIG. 3B. FIG. 5 is an equivalent circuit diagram corresponding to FIGS. 3A and 3B.

In the first embodiment, the compensation structure of the gate-drain parasitic capacitor (C_{gd}) comprises two portions 102a and 102b. The portion 102a of the compensation structure extends to the side 124 of drain D which overlaps pixel electrode 114 from the side 120 of the gate G without connecting to the gate line 102 and the portion 102a partially overlaps side 124 of drain D. The portion 102b of the compensation structure extends to the side 124 of drain D which overlaps pixel electrode 114 from the gate line 102 and the portion 102b partially overlaps side 124 of drain D. Moreover, the other side 122 of the drain D overlaps gate G.

Referring to FIG. 3B and 4, the dotted line indicates a situation in which no alignment shift occurs between M1 and M2 and the solid line indicates a situation after alignment shift has occurred. When the capacitance of parasitic capacitor C_A is changed due to alignment shift, it can be compensated by the parasitic capacitors C_B and C_C. Here,

the capacitance of the gate-drain parasitic capacitor (C_{gd}) is equal to the sum of the capacitance of the parasitic capacitors C_A, C_B, C_C ($C_{gd} = C_A + C_B + C_C$) and $\Delta C_1 + \Delta C_2 \cong 0$. The parasitic capacitor C_A may be a stacked structure comprising a gate insulating layer 104, a semiconductor layer 106, and a channel protection layer 108 or a stacked structure comprising a gate insulating layer 104 and a semiconductor layer 106. The parasitic capacitors C_B and C_C may comprise the gate insulating layer 104 and the semiconductor layer 106. In this embodiment, the drain D may comprise a drain electrode 112D and a drain semiconductor region 110D. Moreover, the source S may comprise a source electrode 112S and a source semiconductor region 110S. The semiconductor layer 106 is used as a channel region for a thin film transistor and may comprise an amorphous silicon layer. The source semiconductor region 110S and the drain semiconductor region 110D may comprise a doped amorphous silicon layer.

It is noted that the compensation structure 102a and 102b are necessary to compensate the capacitance of the gate-drain parasitic capacitor (C_{gd}) within the acceptable alignment shift range between M1 and M2.

FIG. 6 is a plane view of a C_{gd} capacitance-compensated structure according to the second embodiment of the invention. In FIG. 6, the dotted line indicates a situation in which no alignment shift occurs between M1 and M2 and the solid line indicates a situation after alignment shift has occurred.

In the second embodiment, the compensation structure 102a for the gate-drain parasitic capacitor (C_{gd}) extends to

the side 124 of drain D which overlaps pixel electrode 114 from the side 120 of the gate G without connecting to the gate line 102 and the compensation structure 102a partially overlaps side 124 of drain D. When the capacitance of

5 parasitic capacitor C_A is changed due to alignment shift, it can be compensated by the parasitic capacitor C_c. Here, the capacitance of the gate-drain parasitic capacitor (C_{gd}) is equal to the sum of the capacitance of the parasitic capacitors C_A and C_c ($C_{gd} = C_A + C_c$) and $\Delta C_1 + \Delta C_2 \cong 0$.

10   It is noted that two factors must be considered when designing the compensation structure 102a. One factor is the length of the compensation structure 102a depends on the acceptable alignment shift range W_s between M1 and M2. The second factor is the width W of the compensation structure

15 102a depends on the differential capacitance ΔC_1. That is, the length of the compensation structure 102a must be long enough to overlap the drain within the acceptable alignment shift range W_s between M1 and M2, thereby producing a compensative capacitance ΔC_2. Moreover, the width W of the

20 compensation structure 102a must be suitably adjustable to ensure that the modulus of ΔC_2 is substantially equal to that of ΔC_1 ($\Delta C_1 + \Delta C_2 \cong 0$ or $|\Delta C_1| - |\Delta C_2| \cong 0$).

FIG. 7 is a plane view of a C_{gd} capacitance-compensated structure according to the third embodiment of the

25 invention. In FIG. 7, the dotted line indicates a situation in which no alignment shift between M1 and M2 and the solid line indicates a situation after alignment shift has occurred.

In the third embodiment, the compensation structure

30 102b for the gate-drain parasitic capacitor (C_{gd}) extends to

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side 124 of drain D which overlaps pixel electrode 114 from the gate line 102 and the compensation structure 102b partially overlaps side 124 of drain D. When the capacitance of parasitic capacitor C_A is changed due to

5 alignment shift, it can be compensated by the parasitic capacitor C_B. Here, the capacitance of the gate-drain parasitic capacitor (C_{gd}) is equal to the sum of the capacitance of the parasitic capacitors C_A and C_B (C_{gd} = C_A + C_B) and ΔC_1 + $\Delta C_2 \cong 0$.

10 According to the invention, both sides of the drain respectively overlap with the gate and the compensation structure, thereby compensating change of the capacitance of the gate-drain parasitic capacitor due to alignment shift between M1 and M2. Moreover, a parasitic capacitor is

15 formed between one side of the drain and the gate and an additional parasitic capacitor is formed on the other side of the drain to connect to the gate. When the capacitance of the parasitic capacitor formed in the overlapping region between the drain and the gate is changed, it can be

20 compensated by the additional parasitic capacitor formed on the other side of the drain. As a result, the capacitance of the gate-drain parasitic capacitor can be maintained without changing. Accordingly, the liquid crystal display device of the invention can prevent the capacitance of the

25 gate-drain parasitic capacitor form changed due to alignment shift between M1 and M2, thereby increasing yield.

While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the

30 disclosed embodiments. To the contrary, it is intended to

cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such

5 modifications and similar arrangements.